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Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

| Office Action Summary | Application No. 09/981,954 | Applicant(s) MEHTA ET AL. |
|---|---|---|
| | Examiner Kandasamy Thangavelu | Art Unit 2123 |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *18 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1-49 of the application have been examined.

### *Drawings*

2. The drawings submitted on October 18, 2001 are accepted.

### *Specification*

3. The disclosure is objected to because of the following informalities:

Page 15, Lines 1-3, "there is a corresponding memory instance in the first parametric dataset 102B that is actually simulated" appears to be incorrect and it appears that it should be "there is a corresponding memory instance in the first parametric dataset 102A that is actually simulated".

Appropriate correction is required.

### *Claim Rejections - 35 USC § 101*

4. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. Claims 46-49 are rejected under 35 U.S.C. 101 because the claimed inventions are directed to non-statutory subject matter.

5.1 Computer accessible medium claims 46-49 are rejected for not specifying in the specification what the computer accessible medium is, thus allowing wide interpretation of this term including carrier wave, hard disk, floppy disk, compact disk, memory boards etc. While the computer accessible medium of hard disk, floppy disk, compact disk, memory boards etc. is statutory, the carrier wave is not statutory.

6.1 Claims 46-49 would be **statutory** be specifying in the specification what the computer accessible medium is and what it stores; the computer accessible medium should not include carrier wave.

## ***Claim Interpretations***

7. The claims have been interpreted using the following interpretations of the terms memory compiler, memory instance, congruent memory instance and scale factors:

There are two different uses of the term "memory compiler" in vogue in the IC design world. One is that memory compiler is **a program** that generates various configurations of the memory such as ROM, DRAM, SRAM, EPROM, flash memory etc. to meet the user specifications. Each **memory configuration** generated is called as **memory instance**. The program generates a file which is used as input to simulate the memory configuration and

evaluate the performance. See **Ellis et al.** (U.S. Patent 6,538,932) CL1, L12-16. Another use of "memory compiler" refers to **a framework or macro** encapsulating various representations of the memory design database to ease exploring the design database. Here the "memory compiler" contains the **data specifications** for some memory instances. See **Lim et al.** ("A widely configurable EPROM memory compiler for embedded applications, IEEE, 1998) Page 1, CL1, Para 1, L1-5.

The specification states at Page 4, L1-3, "each particular compiler that corresponds to an instance needs to be characterized with respect to several key parameters". Therefore the memory compiler contains the **data defining key parameters** of the memory instance. The specification also states at Page 4, L11-12, "a memory compiler is associated with each instance of a particular row/column combination" and at Lines 23-26, "the memory compilers' **parametric data** generated via characterization must be within a narrow range of the actual data obtained for the corresponding memory instances". Specification states at Page 5, L13-15, "where migration to a different family of compilers is necessitated due to a change in the MUX factor or adaptation of a different technology, an entirely new set of memory compilers needs to be characterized". Hence, the application and the claims use the term "memory compiler" to mean

**data specifications** for some memory instances. The claims are interpreted using this definition of the memory compiler.

The term "memory instance" refers to **memory configurations** generated using a memory compiler's parametric data.

Specification Page 6, Lines 11-17 state, "The memory compilers of the second type are matched with the memory compilers of the first type (i.e., congruent), in that a memory compiler of the second type operable to compile a memory instance of i rows and j columns has a corresponding compiler of the first type with the same row and column combination". Therefore, the term "**congruent memory instance**" refers to a memory instance (memory configuration) of the second type that has **same numbers of rows and columns** as the memory instance of the first type.

Specification Page 6, Lines 18-23 state, "Absolute scale factors are determined based on the **ratio of the parametric data points** of two congruent memory compilers, one of each type. Thereafter, interpolated scale factors are obtained based on the absolute scale factors, preferably using a 4-point interpolation technique". Therefore scale factors refer to some **multiplication factors** to obtain the value of a parameter for the second memory instance of the second type from a corresponding (congruent) memory instance of the first type. Interpolated scale factors are **interpolated multiplication factors** that are obtained from basic multiplication factors when 4-point interpolation is used between the memory compilers of the first and second types.

These definitions of memory instance, congruent memory instance and scale factors are used in the interpretation of the claims.

## *Claim Rejections - 35 USC § 102*

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

9. Claims 1, 5-15, 35-38, 45-47 and 49 are rejected under 35 U.S.C. § 102(e) as being anticipated by **Djaja et al.** (U.S. Patent 6,405,160).

9.1 **Djaja et al.** teaches Memory compiler interface and methodology. Specifically, as per claim 1, **Djaja et al.** teaches a memory compiler characterization method for determining parametric data associated with compilable memory instances (Abstract, L1-8; Fig. 2, Item 70; CL1, L5-12; Fig. 4; CL1, L55-57; CL4, L64-67), comprising the steps:

obtaining a first parametric dataset for a first plurality of memory compilers, each of the memory compilers for compiling a respective memory instance having a select number of physical rows and a select number of physical columns (Abstract, L1-8; CL1, L31-34; CL2, L16-27; CL5, L13-20), wherein each memory instance is organized using a first MUX factor and each data point in the first parametric dataset corresponds to the respective memory instance (Abstract, L1-8; CL5, L13-20), the data point comprising a value with respect to a particular parameter (Abstract, L6-8; CL5, L13-20);

obtaining a second parametric dataset by characterizing the particular parameter for a second plurality of memory compilers (Abstract, L1-8; Fig. 2, Item 70; CL1, L31-34), each of the second plurality of memory compilers for compiling a respective memory instance organized with a second MUX factor (Abstract, L1-4 and L6-8), wherein the second plurality of memory compilers are sampled from the first plurality of memory compilers such that each memory instance compiled by the second plurality of memory compilers corresponds to a respective congruent memory instance of the first parametric dataset having identical numbers of physical rows and physical columns (Fig. 4, bottom plane at MUX of 2 and top plane at MUX of 16; CL5, L2-12; CL5, L13-20; CL5, L28-31);

determining scale factors for a select number of parametric data points associated with respective congruent memory instances of the first and second parametric datasets (Fig. 4, corner vertical lines; CL2, L46-47; CL4, L64-67; CL5, L52-65);

obtaining an interpolated scale factor based on the scale factors (Fig. 4, the lines defining the horizontal plane in the middle of the cubicle); and

deriving a value of the particular parameter for an additional memory instance of second parametric dataset by applying the interpolated scale factor to a data point associated with a memory instance of the first parametric dataset, wherein the memory instance is congruent with respect to the additional memory instance of the second parametric dataset (Fig. 4, the lines defining the horizontal plane in the middle of the cubicle).

Per claims 5 and 6: **Djaja et al.** teaches that the first MUX factor is selected from the group consisting of a MUX-4 factor, a MUX-8 factor, a MUX-16 factor and a MUX-32 factor;

and the second MUX factor is selected from the group consisting of a MUX-4 factor, a MUX-8 factor, a MUX-16 factor and a MUX-32 factor (CL5, L28-31; Fig. 4).

Per claims 7-11: **Djaja et al.** teaches that each memory instance of the first and second parametric datasets comprises a read-only memory (ROM) circuit; each memory instance of the first and second parametric datasets comprises a static random access memory (SRAM) circuit; each memory instance of the first and second parametric datasets comprises a dynamic random access memory (DRAM) circuit; each memory instance of the first and second parametric datasets comprises an electrically programmable ROM (EPROM) circuit; and each memory instance of the first and second parametric datasets comprises a flash memory circuit (CL1, L5-12).

Per claim 12: **Djaja et al.** teaches that each memory instance of the first and second parametric datasets comprises an embedded memory circuit (CL2, L12-14).

Per claim 13: **Djaja et al.** teaches that each memory instance of the first and second parametric datasets comprises a stand-alone memory circuit (Abstract, L1-8; CL1, L5-12).

Per claim 14: **Djaja et al.** teaches that the interpolated scale factor is obtained by interpolating four scale factors, each corresponding to a ratio of values of the particular parameter for a pair of congruent memory instances (Fig. 4, the lines defining the horizontal plane in the middle of the cubicle).

Per claim 15: **Djaja et al.** teaches that the step of obtaining the first parametric dataset and the step of obtaining the second parametric dataset are effectuated by characterization of the particular parameter via simulation (Fig. 2, Items 70, 72b; CL2, L10-12; CL5, L47-49).

9.2 As per claim 35, **Djaja et al.** teaches a memory compiler characterization system (Abstract, L1-8; Fig. 2, Item 70; CL1, L5-12; Fig. 4; CL1, L55-57; CL4, L64-67), comprising:

means for characterizing a first plurality of memory compilers with respect to a particular parameter, the first plurality of memory compilers for compiling memory instances of a first type (Abstract, L1-8; CL1, L31-34; CL2, L16-27; CL5, L13-20);

means for characterizing a second plurality of memory compilers with respect to the particular parameter, the second plurality of memory compilers for compiling memory instances of a second type (Abstract, L1-8; Fig. 2, Item 70; CL1, L31-34), wherein the memory instances of second type comprise memory instances sparsely sampled from the memory instances of first type such that each memory instance of second type corresponds to a respective congruent memory instance of first type having identical numbers of physical rows and physical columns (Fig. 4, bottom plane at MUX of 2 and top plane at MUX of 16; CL5, L2-12; CL5, L13-20; CL5, L28-31);

means for determining scale factors between values of the particular parameter respectively associated with a sample of congruent memory instances of the first and second types (Fig. 4, corner vertical lines; CL2, L46-47; CL4, L64-67; CL5, L52-65);

an interpolator to obtain an interpolated scale factor based on the scale factors (Fig. 4, the lines defining the horizontal plane in the middle of the cubicle); and

means for obtaining a value of the particular parameter for an additional memory instance of second type by utilizing the interpolated scale factor in conjunction with a parametric value of a congruent memory instance of first type which corresponds to the additional memory instance (Fig. 4, the lines defining the horizontal plane in the middle of the cubicle).

Per claims 36, 37 and 38: **Djaja et al.** teaches that the memory instances of first type comprise memory instances with a first MUX factor and the memory instances of second type comprise memory instances with a second MUX factor; the first MUX factor is selected from the group consisting of a MUX-4 factor, a MUX-8 factor, a MUX-26 factor and a MUX-32 factor; and the second MUX factor is selected from the group consisting of a MUX-4 factor, a MUX-8 factor, a MUX-7.6 factor and a MUX-32 factor (CL5, L28-31; Fig. 4).

Per claim 45: **Djaja et al.** teaches that the memory instances comprise one of a DRAM circuit, an SRAM circuit, a ROM circuit, an EPROM circuit and a flash memory circuit (CL1, L5-12).

9.3 As per Claims 46 and 47, these are rejected based on the same reasoning as Claims 35 and 36, supra. Claims 46 and 47 are computer-accessible medium claims reciting the same limitations as Claims 35 and 36, as taught throughout by **Djaja et al.**

9.4 As per Claim 49, it is rejected based on the same reasoning as Claims 45, supra. Claim 49 is a computer-accessible medium claim reciting the same limitations as Claim 45, as taught throughout by **Djaja et al.**

## ***Claim Rejections - 35 USC § 103***

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

11. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

12. Claims 2-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Djaja et al.** (U.S. Patent 6,405,160) in view of **Yuan et al.** (U.S. Patent 6,249,901).

12.1 As per claim 2, **Djaja et al.** teaches the method of claim 1. **Djaja et al.** does not expressly teach that the particular parameter comprises a memory timing parameter. **Yuan et al.** teaches that the particular parameter comprises a memory timing parameter (Abstract, L1-3 and L7-11; Fig. 3; Fig. 5, Items 214, 236 and 244; Fig. 6B, Items 272, 290; Fig. 6D, Items 272, 304, 310 and 312; CL2, L8-35), because that allows the IC designers to optimize the memory timing parameters to increase the performance of the memory circuit (CL2, L5-7; CL5, L37-39); and the memory characterization method provides improved accuracy in determining the timing characteristics and generates a large number of memory instances of a memory compiler in a relatively short period of time (CL5, L65-67; CL6, L58-62). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Djaja et al.** with the method of **Yuan et al.** that included the particular parameter comprising a memory timing parameter. The artisan would have been motivated because that would allow the IC designers to optimize the memory timing parameters to increase the performance of the memory circuit; and the memory characterization method would provide improved accuracy in determining the timing characteristics and generate a large number of memory instances of a memory compiler in a relatively short period of time.

12.2 As per claims 3 and 4, **Djaja et al.** and **Yuan et al.** teach the method of claim 2. **Djaja et al.** does not expressly teach that the memory timing parameter comprises memory access time; and the memory timing parameter comprises memory cycle time. **Yuan et al.** teaches that the memory timing parameter comprises memory access time; and the memory timing parameter comprises memory cycle time (CL1, L66 to CL2, L5), because that allows the IC designers to

optimize the memory timing parameters to increase the performance of the memory circuit (CL2, L5-7; CL5, L37-39); and the memory characterization method provides improved accuracy in determining the timing characteristics and generates a large number of memory instances of a memory compiler in a relatively short period of time (CL5, L65-67; CL6, L58-62). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Djaja et al.** with the method of **Yuan et al.** that included the memory timing parameter comprising memory access time; and the memory timing parameter comprising memory cycle time. The artisan would have been motivated because that would allow the IC designers to optimize the memory timing parameters to increase the performance of the memory circuit; and the memory characterization method would provide improved accuracy in determining the timing characteristics and generate a large number of memory instances of a memory compiler in a relatively short period of time.

13. Claims 16, 20-34, 39-44 and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Djaja et al.** (U.S. Patent 6,405,160) in view of **Murotani** (U.S. Patent 5,175,707).

13.1 As per claim 16, **Djaja et al.** teaches a memory compiler characterization method for determining parametric data associated with compilable memory instances (Abstract, L1-8; Fig. 2, Item 70; CL1, L5-12; Fig. 4; CL1, L55-57; CL4, L64-67), comprising the steps:

obtaining a first parametric dataset for a first plurality of memory compilers, each of the memory compilers for compiling a respective memory instance having a select number of

physical rows and a select number of physical columns (Abstract, L1-8; CL1, L31-34; CL2, L16-27; CL5, L13-20), and organized using a select MUX factor wherein each data point in the first parametric dataset corresponds to the respective memory instance (Abstract, L1-8; CL5, L13-20), the data point comprising a value with respect to a particular parameter (Abstract, L6-8; CL5, L13-20);

obtaining a second parametric dataset by characterizing the particular parameter for a second plurality of memory compilers (Abstract, L1-8; Fig. 2, Item 70; CL1, L31-34), each of the second plurality of memory compilers for compiling a respective memory instance organized with a second MUX factor (Abstract, L1-4 and L6-8), wherein the second plurality of memory compilers are sampled from the first plurality of memory compilers such that each memory instance compiled by the second plurality of memory compilers corresponds to a respective congruent memory instance of the first parametric dataset having identical numbers of physical rows and physical columns (Fig. 4, bottom plane at MUX of 2 and top plane at MUX of 16; CL5, L2-12; CL5, L13-20; CL5, L28-31);

determining scale factors for a select number of parametric data points associated with respective congruent memory instances of the first and second parametric datasets (Fig. 4, corner vertical lines; CL2, L46-47; CL4, L64-67; CL5, L52-65);

obtaining an interpolated scale factor based on the scale factors (Fig. 4, the lines defining the horizontal plane in the middle of the cubicle); and

deriving a value of the particular parameter for an additional memory instance of second parametric dataset by applying the interpolated scale factor to a data point associated with a memory instance of the first parametric dataset, wherein the memory instance is congruent with

respect to the additional memory instance of the second parametric dataset (Fig. 4, the lines defining the horizontal plane in the middle of the cubicle).

**Djaja et al.** does not expressly teach that the first plurality of memory compilers are representative of a first memory technology; and the second plurality of memory compilers are representative of a second memory technology. **Murotani** teaches that the first plurality of memory compilers are representative of a first memory technology; and the second plurality of memory compilers are representative of a second memory technology (CL1, L20-26), because the memory technology selected depends on the size and capacity of the memory required for the application (CL1, L20-26). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Djaja et al.** with the method of **Murotani** that included the first plurality of memory compilers being representative of a first memory technology; and the second plurality of memory compilers being representative of a second memory technology. The artisan would have been motivated because the memory technology selected would depend on the size and capacity of the memory required for the application.

Per claim 20: **Djaja et al.** teaches that the select MUX factor is selected from the group consisting of a MUX-4 factor, a MUX-8 factor, a MUX-16 factor and a MUX-32 factor (CL5, L28-31; Fig. 4).

Per claims 21-25: **Djaja et al.** teaches that each memory instance of the first and second parametric datasets comprises a read-only memory (ROM) circuit; each memory instance of the

first and second parametric datasets comprises a static random access memory (SRAM) circuit; each memory instance of the first and second parametric datasets comprises a dynamic random access memory (DRAM) circuit; each memory instance of the first and second parametric datasets comprises an electrically programmable ROM (EPROM) circuit; and each memory instance of the first and second parametric datasets comprises a flash memory circuit (CL1, L5-12).

Per claim 26: **Djaja et al.** teaches that each memory instance of the first and second parametric datasets comprises an embedded memory circuit (CL2, L12-14).

Per claim 27: **Djaja et al.** teaches that each memory instance of the first and second parametric datasets comprises a stand-alone memory circuit (Abstract, L1-8; CL1, L5-12).

Per claim 28: **Djaja et al.** teaches that the interpolated scale factor is obtained by interpolating four scale factors, each corresponding to a ratio of values of the particular parameter for a pair of congruent memory instances (Fig. 4, the lines defining the horizontal plane in the middle of the cubicle).

Per claim 29: **Djaja et al.** teaches that the step of obtaining the first parametric dataset and the step of obtaining the second parametric dataset are effectuated by characterization of the particular parameter via simulation (Fig. 2, Items 70, 72b; CL2, L10-12; CL5, L47-49).

13.2 As per claims 30 and 31, **Djaja et al.** and **Murotani** teach the method of claim 16. **Djaja et al.** does not expressly teach that the first memory technology is selected from the group consisting of 1.0 μ technology, 0.8 μ technology, 0.6 μ technology and 0.2 μ technology; and the second memory technology is selected from the group consisting of 1.0 μ technology, 0.8 μ technology, 0.6 μ technology and 0.2 μ technology. **Murotani** teaches that the first memory technology is selected from the group consisting of 1.0 μ technology, 0.8 μ technology, 0.6 μ technology and 0.2 μ technology; and the second memory technology is selected from the group consisting of 1.0 μ technology, 0.8 μ technology, 0.6 μ technology and 0.2 μ technology (CL1, L20-26), because the memory technology selected depends on the size and capacity of the memory required for the application (CL1, L20-26). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Djaja et al.** with the method of **Murotani** that included the first memory technology being selected from the group consisting of 1.0 μ technology, 0.8 μ technology, 0.6 μ technology and 0.2 μ technology; and the second memory technology being selected from the group consisting of 1.0 μ technology, 0.8 μ technology, 0.6 μ technology and 0.2 μ technology. The artisan would have been motivated because the memory technology selected would depend on the size and capacity of the memory required for the application.

13.3 As per claim 32, **Djaja et al.** and **Murotani** teach the method of claim 16. **Djaja et al.** does not expressly teach that the first and second memory technologies comprise design rule-specific technologies. **Murotani** teaches that the first and second memory technologies comprise design rule-specific technologies (CL1, L20-26), because the memory technology

selected depends on the size and capacity of the memory required for the application (CL1, L20-26). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Djaja et al.** with the method of **Murotani** that included the first and second memory technologies comprising design rule-specific technologies. The artisan would have been motivated because the memory technology selected would depend on the size and capacity of the memory required for the application.

Per claims 33 and 34: **Djaja et al.** teaches that the first and second memory technologies comprise foundry specific technologies; and the first and second memory technologies comprise process flow-specific technologies (CL2, L16-19).

13.4 As per claim 39, **Djaja et al.** teaches the system of claim 35. **Djaja et al.** does not expressly teach that the memory instances of first type comprise memory instances associated with a first memory technology and the memory instances of second type comprise memory instances associated with a second memory technology. **Murotani** teaches that the memory instances of first type comprise memory instances associated with a first memory technology and the memory instances of second type comprise memory instances associated with a second memory technology (CL1, L20-26), because the memory technology selected depends on the size and capacity of the memory required for the application (CL1, L20-26). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Djaja et al.** with the system of **Murotani** that included the memory instances of first type comprising memory instances associated with a first memory technology and the memory

instances of second type comprising memory instances associated with a second memory technology. The artisan would have been motivated because the memory technology selected would depend on the size and capacity of the memory required for the application.

13.5 As per claims 40 and 41, **Djaja et al.** and **Murotani** teach the system of claim 39. **Djaja et al.** does not expressly teach that the first memory technology is selected from the group consisting of 1.0 μ technology, 0.8 μ technology, 0.6 μ technology and 0.2 μ technology; and the second memory technology is selected from the group consisting of 1.0 μ technology, 0.8 μ technology, 0.6 μ technology and 0.2 μ technology. **Murotani** teaches that the first memory technology is selected from the group consisting of 1.0 μ technology, 0.8 μ technology, 0.6 μ technology and 0.2 μ technology; and the second memory technology is selected from the group consisting of 1.0 μ technology, 0.8 μ technology, 0.6 μ technology and 0.2 μ technology (CL1, L20-26), because the memory technology selected depends on the size and capacity of the memory required for the application (CL1, L20-26). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Djaja et al.** with the system of **Murotani** that included the first memory technology being selected from the group consisting of 1.0 μ technology, 0.8 μ technology, 0.6 μ technology and 0.2 μ technology; and the second memory technology being selected from the group consisting of 1.0 μ technology, 0.8 μ technology, 0.6 μ technology and 0.2 μ technology. The artisan would have been motivated because the memory technology selected would depend on the size and capacity of the memory required for the application.

13.6 As per claim 42, **Djaja et al.** and **Murotani** teach the system of claim 35. **Djaja et al.** does not expressly teach that the first and second memory technologies comprise design rule-specific technologies. **Murotani** teaches that the first and second memory technologies comprise design rule-specific technologies (CL1, L20-26), because the memory technology selected depends on the size and capacity of the memory required for the application (CL1, L20-26). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Djaja et al.** with the system of **Murotani** that included the first and second memory technologies comprising design rule-specific technologies. The artisan would have been motivated because the memory technology selected would depend on the size and capacity of the memory required for the application.

Per claims 43 and 44: **Djaja et al.** teaches that the first and second memory technologies comprise foundry specific technologies; and the first and second memory technologies comprise process flow-specific technologies (CL2, L16-19).

13.7 As per Claim 48, it is rejected based on the same reasoning as Claims 39, supra. Claim 48 is a computer-accessible medium claim reciting the same limitations as Claim 39, as taught throughout by **Djaja et al.** and **Murotani.**

14. Claims 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Djaja et al.** (U.S. Patent 6,405,160) in view of **Murotani** (U.S. Patent 5,175,707), and further in view of **Yuan et al.** (U.S. Patent 6,249,901).

14.1 As per claim 17, **Djaja et al.** and **Murotani** teach the method of claim 16. **Djaja et al.** does not expressly teach that the particular parameter comprises a memory timing parameter. **Yuan et al.** teaches that the particular parameter comprises a memory timing parameter (Abstract, L1-3 and L7-11; Fig. 3; Fig. 5, Items 214, 236 and 244; Fig. 6B, Items 272, 290; Fig. 6D, Items 272, 304, 310 and 312; CL2, L8-35), because that allows the IC designers to optimize the memory timing parameters to increase the performance of the memory circuit (CL2, L5-7; CL5, L37-39); and the memory characterization method provides improved accuracy in determining the timing characteristics and generates a large number of memory instances of a memory compiler in a relatively short period of time (CL5, L65-67; CL6, L58-62). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Djaja et al.** with the method of **Yuan et al.** that included the particular parameter comprising a memory timing parameter. The artisan would have been motivated because that would allow the IC designers to optimize the memory timing parameters to increase the performance of the memory circuit; and the memory characterization method would provide improved accuracy in determining the timing characteristics and generate a large number of memory instances of a memory compiler in a relatively short period of time.

14.2 As per claims 18 and 19, **Djaja et al.**, **Murotani** and **Yuan et al.** teach the method of claim 2. **Djaja et al.** does not expressly teach that the memory timing parameter comprises memory access time; and the memory timing parameter comprises memory cycle time. **Yuan et al.** teaches that the memory timing parameter comprises memory access time; and the memory

timing parameter comprises memory cycle time (CL1, L66 to CL2, L5), because that allows the IC designers to optimize the memory timing parameters to increase the performance of the memory circuit (CL2, L5-7; CL5, L37-39); and the memory characterization method provides improved accuracy in determining the timing characteristics and generates a large number of memory instances of a memory compiler in a relatively short period of time (CL5, L65-67; CL6, L58-62). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Djaja et al.** with the method of **Yuan et al.** that included the memory timing parameter comprising memory access time; and the memory timing parameter comprising memory cycle time. The artisan would have been motivated because that would allow the IC designers to optimize the memory timing parameters to increase the performance of the memory circuit; and the memory characterization method would provide improved accuracy in determining the timing characteristics and generate a large number of memory instances of a memory compiler in a relatively short period of time.

## *Conclusion*

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 571-272-3717. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard, can be reached on 571-272-3749. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K. Thangavelu
Art Unit 2123
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